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To: **Examiner: DIEP, Nhon T.**
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Number of Pages: Cover + 2

From: Caroline T. Do, Esq.
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Re: U.S. Patent Application Serial No.:
09/974,530
Filing Date: October 10, 2001
Title: MULTISTANDARD VIDEO
DECODER AND DECOMPRESSION
SYSTEM FOR PROCESSING ENCODED
BIT STREAMS INCLUDING A VIDEO
FORMATTER AND METHODS RELATING
THERETO
Confirmation No.: 1318
Art Unit: 2613
Inventor: Adrian P. Wise et al.
Attorney Docket No.:
94100423(EP)USC1X1C1D7D1 PDDD

Examiner Diep's Fax: 1 (571) 273-7328

PLEASE CONTACT US IF ANY PAGES ARE
ILLEGIBLE OR ARE NOT RECEIVED

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Dear Examiner Diep:

Further to our facsimile dated February 26, 2007 regarding page 65, please delete lines 9, 10, 11 (For ease of reference, the various .... output signals:) to match with lines 35-53 of Column 41 as indicated on U.S. Patent 6,435,737 B1 (Application # 08/482,296, filed June 7, 1995). Both copies are attached herewith for your reference.

Thank you for your patience and kindly acknowledge receipt by a return fax.

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interface according to this embodiment can be adapted very easily to different applications.

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The duplication stage shown in Fig. 8 also has two latches LEIN and LEOUT that, as in the example shown in Fig. 6, latch the state of the extension bit at the input and at the output of the stage, respectively. As Fig. 8a shows, the input extension latch LEIN is clocked synchronously with the input data latch LDIN and the validation signal IN_VALID.

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For ease of reference, the various latches included in the duplication stage are paired below with their respective output signals:

delete this Paragraph

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In the duplication stage, the output from the data latch LDIN forms intermediate data referred to as MID_DATA. This intermediate data word is loaded into the data output latch LDOUT only when an intermediate acceptance signal (labeled "MID_ACCEPT" in Fig. 8a) is set HIGH.

The portion of the circuitry shown in Fig. 8 below the acceptance latches LAIN, LAOUT, shows the circuits that are added to the basic pipeline structure to generate the various